

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A register controlled delay locked loop (DLL) using a comparison reference clock and a delay monitoring clock which are a internal clock internal clocks synchronized with an external clock ~~as a delay monitoring clock and a comparison reference clock~~, the register controlled delay locked loop (DLL) comprising:

a first delay line having a plurality of sub delay chains grouped with a plurality of delay units for receiving the internal clock;

a second delay line having a plurality of sub delay chains grouped with a plurality of delay units and receiving the delay monitoring clock and generating a second delayed clock;

a delay model for generating a delay model signal by reflecting a delay condition of a real clock path on the second delayed clock from the second delay line;

a phase comparison means for generating a phase comparison signal by comparing a phase of the comparison reference clock with the delay model signal from the delay model;

a shift register control means for generating a shift control signal by responding to the phase comparison signal from the phase comparison means;

a master shift register for selecting one of the sub delay chains of the first delay line and the second delay line by responding to the shift control signal; and

a slave shift register for selecting one of the delay units in the sub delay chain selected by the master shift register according to the shift control signal.

2. (Currently Amended) The register controlled DLL as recited in claim 1, further comprising:

a clock dividing means for generating the delay monitoring clock and the comparison ~~standard~~ reference clock by dividing the internal clock.

3. (Original) The register controlled DLL as recited in claim 1, further comprising:

a DLL driving means for generating a DLL clock by receiving the first delayed signal from the first delay chain at a delay locking.

4. (Original) The register controlled DLL as recited in claim 1, wherein the master shift register and the slave shift register

are independently operated, respectively.

5. (Original) The register controlled DLL as recited in claim 4, wherein the master shift register and the slave shift register performs a shift operation in opposite directions, respectively.

6. (Currently Amended) A register controlled delay locked loop (DLL) using a comparison reference clock and a delay monitoring clock which are ~~a internal clock~~ internal clocks synchronized with an external clock ~~as a delay monitoring clock and a comparison reference clock~~, comprising:

a first delay line having a plurality of sub delay chains grouped with a plurality of slave delay units and one master delay unit for receiving the internal clock and generating a first delay signal;

a second delay line having a plurality of sub delay chains grouped with a plurality of slave delay units and one master delay unit for receiving the delay monitoring clock as the input and generating a second delay signal;

a delay model for generating a delay model signal by reflecting a delay condition of a real clock path on the second delayed signal from the second delay line;

a phase comparison means for comparing a phase of the comparison reference clock with the delay model signal from the delay model and generating a phase comparison signal;

a shift register control means for generating a shift control signal by responding to the phase comparison signal from the phase comparison means;

a master shift register for selecting one among the master delay units of the first delay line and the second delay line by responding to the shift control signal; and

a slave shift register for selecting one of the slave delay units in the sub delay chain selected by the master shift register by responding to the shift control signal.

7. (Original) The register controlled DLL as recited in claim 6, further comprising:

a clock dividing means for generating the delay monitoring clock and the comparison standard clock by dividing the internal clock.

8. (Original) The register controlled DLL as recited in claim 6, further comprising:

a DLL driving means for generating a DLL clock by receiving the first delayed signal from the first delay chain at a delay locking.

9. (Original) The register controlled DLL as recited in claim 6, wherein the master delay unit is disposed at a hindmost part of the sub delay chain and a front of the master delay unit.

10. (Original) The register controlled DLL as recited in claim 9, wherein the master shift register and the slave shift register are independently operated, respectively.

11. (Original) The register controlled DLL as recited in claim 10, wherein the master shift register performs a shift right operation and the slave shift register performs a shift left operation at an initial mode.

12. (Original) The register controlled DLL as recited in claim 9, wherein the master shift register has same number of stages as the number of the sub delay chains.

13. (Original) The register controlled DLL as recited in claim 12, wherein the slave shift register has same number of stages as the number of the slave delay units in one of the sub delay chains and an output of the slave shift register is commonly used for each sub delay chain.

14. (Original) The register controlled DLL as recited in claim 13, wherein the shift register control means includes a shift right/left control unit for controlling a shift operation of the master shift register and the slave shift register by responding to the phase comparison signal.

15. (Original) The register controlled DLL as recited in claim 14, wherein the shift register control means includes a master delay unit disable signal generation unit for generating the master delay unit disable signal by responding to the shift control signal for controlling the shift right/left operation of the master shift register.

16. (Original) The register controlled DLL as recited in claim 15, wherein the master delay unit in each sub delay chain is controlled by an output of the master shift register and the master delay unit disable signal.

17. (Original) The register controlled DLL as recited in claim 16, wherein the slave delay chain in each sub delay chain is controlled by the output of the master shift register for selecting the master delay unit of the corresponding sub delay chain.

18. (Original) The register controlled DLL as recited in claim 15, wherein the shift register control means includes a master/slave signal passing control unit for providing an interlocking between the master delay unit and the slave delay unit adjacent to the master delay unit during a delay re-adjustment after the delay locking is completed by the initial operation.

19. (Original) The register controlled DLL as recited in claim 18, wherein the master/slave signal passing control unit generates the phase comparison signal, the output of the slave shift register for selecting a first slave delay unit, the output of the slave shift register for selecting a last slave delay unit, a master shifting enable signal by responding to the master delay unit disable signal, the slave shifting enable signal, a slave shifting enable signal, a slave shift register set signal, and a slave shift register reset signal.

20. (Original) The register controlled DLL as recited in claim 19, wherein the shift right/left control unit is controlled by the master shifting enable signal and the slave shifting enable signal.